CLAIM REJECTIONS

REMARKS

Claims 1-6 are pending. Claim 1 is amended herein. Claim 10 is cancelled herein. No new matter has been added as a result of the amendments.

35 U.S.C. §103 Rejections

Claims 6-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kloen et al. (WO 00/350013), hereinafter referred to as Kloen, in combination with Thakur et al. (US Publication 2006/0030162), hereinafter referred to as Thakur.

The Examiner is respectfully directed to currently amended independent Claim 1, which recites a semiconductor structure comprising:

a substrate;

a pad area wherein said pad area comprises:

a first layer of metal disposed directly above said substrate, wherein said first layer of metal is in immediate physical contact with said substrate;

a second layer of metal disposed above said first layer of metal;

a layer of dielectric disposed between said first metal layer and said

secondmetal layer;

a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer; and

one or more subsequent layers of metal between said first and said second metal layers, wherein said via comprises one or more of a plurality of vias and wherein one or more of said vias electrically couples one or more of said subsequent layers with one or more of each other, said first and said second layers of metal; and

an active device of said semiconductor structure disposed in said substrate, wherein said active device is not physically separated from said pad area by a material other than said substrate where said active device resides.

Claims 2-6 depend from currently amended independent Claim 1 and recite further limitations of the claimed invention. Applicant respectfully asserts that the present invention is neither shown nor suggested by the Kloen reference or the Thakur reference alone or in combination.

Conventionally, a pad area is separate from active circuits in a chip. Specifically, active devices can not be present within the substrate that is directly beneath a typical pad. In contrast to traditional approaches, embodiments of the claimed subject matter, in one example, are directed towards developing a more efficient use of silicon areas without compromising chip performance by designing pad areas that allow active

devices to operate immediately underneath. In one instance, embodiments set forth a semiconductor structure where an active device implanted in a substrate directly in contact with a pad area is able to operate properly.

The Kloen reference, on the other hand, is directed towards providing an integrated circuit device that can withstand the forces exerted during wirebonding and counteract the occurrence of damage to the active circuit without an increase in device and process complexity (page 2, lines 9-13).

The Kloen reference does not teach or show an active circuit operating in a substrate that is directly beneath a pad. Kloen teaches away from this by showing a plurality of bond pads (3) to be situated above a passivating material that does not have any active circuits within. Kloen shows the active circuits to be underneath and shielded by the passivating material. In particular, the purpose served by the passivating material is to serve as a buffer zone in order to counteract the possible occurrence of damage to the active circuit. (emphasis added)

Nowhere in the Kloen reference is disclosed "a substrate; a pad area wherein said pad area comprises: a first layer of metal disposed directly above said substrate, wherein said first layer of metal is in immediate physical contact with said substrate; a second layer of metal disposed above said first layer of metal; a layer of dielectric disposed

between said first metal layer and said second metal layer; a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer; and one or more subsequent layers of metal between said first and said second metal layers, wherein said via comprises one or more of a plurality of vias and wherein one or more of said vias electrically couples one or more of said subsequent layers with one or more of each other, said first and said second layers of metal; and an active device of said semiconductor structure disposed in said substrate, wherein said active device is not physically separated from said pad area by a material other than said substrate where said active device resides."(emphasis added). Thus, Applicant respectfully reasserts the Kloen reference does not teach the present claimed invention.

Further, Applicant respectfully asserts that the Thakur reference does not overcome the shortcomings of the Kloen reference. Thus, Applicant respectfully reasserts the Kloen reference alone or in combination with the Thakur reference does not teach the present claimed invention.

Therefore, Claim 1 is in condition for allowance. Also, Claims 2-6 overcome the Examiner's prior basis for rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

SUMMARY

In view of the foregoing remarks, the Applicant respectfully submits that the pending claims in the instant patent application are in condition for allowance. The Applicant respectfully requests reconsideration of the Application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact James Hao at the below listed phone number.

Respectfully submitted,

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